Listing of the Claims:

Below is a listing of all claims using a strikethrough and underlining to show changes.

1. (currently amended) A system for ~~handling~~ converting network communications data between multiple communications protocols, the system comprising:

a plurality of programmable processors, each processor having multiple thread units, each thread unit capable of fully executing programs, wherein the thread units ~~within a processor being assigned processing of various protocol functions in a parallel/pipelined fashion~~ are operable for performing communications protocol conversion of data frames, and wherein the processors perform the protocol conversion using parallel processing and pipelined processing; and

a hardwired logic front end connected to a network interface for receiving and transmitting data, said hardwired logic performing time critical operations and communicating received data to and data to be transmitted from said plurality of programmable processors.

2. (original) The system recited in claim 1, wherein each of said programmable processors includes on-chip embedded memory for storing status and control information of current network traffic and for storing received data and data to be transmitted.

3. (original) The system recited in claim 2, said embedded memory contains an area dedicated for packet storage, an area where the payload and headers of frames are stored, an area for storing control and status blocks, an area where various protocol specific information and the current status of the network traffic is stored, and an area for working queues, as well as any other information required.

4. (original) The system recited in claim 3, wherein a beginning address of an inbound data block (IBDB) is added to the master input queue by an input processing unit which manages an IBDB memory area, a "master" thread assigning incoming frames to one of a number of threads performing a network protocol, frame dispatching being performed by a workload allocation function which may include workload balancing functionality.

5. (original) The system recited in claim 2, wherein each of said programmable processors includes an on-chip high-speed interconnect connecting the embedded memory and said multiple thread units.

6. (original) The system recited in claim 5, wherein each of said multiple thread units comprises a register file, a program counter, an arithmetic logic unit (ALU), and logic for instruction fetching, decoding and dispatching.

7. (original) The system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a ring.

8. (original) The system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as dual counter rotating rings.

9. (original) The system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a local bus.

10. (original) The system recited in claim 5, wherein the on-chip high-speed interconnect is implemented as a switch.

11. (original) The system recited in claim 5, further comprising an interprocessor highspeed interconnect connecting said plurality of programmable processors and said hardwired logic front end, and an interconnect interface connecting the on-chip high-speed interconnect of each programmable processor to the interprocessor high-speed interconnect.

12. (currently amended) The system recited in claim 11, wherein said hardwired logic front end comprises:

a receiver and a transmitter connected to port logic, said receiver outputting received frame data according to a first protocol and said transmitter receiving frame data ~~to be transmitted~~ according to the first protocol;

an inbound interface which receives frame data output by said port logic; ~~and~~

an outbound interface which outputs frame data to be transmitted to said port logic, said inbound interface and said outbound interface being connected to said interprocessor high-speed interconnect;

a second receiver and a second transmitter connected to second port logic, said second receiver outputting received frame data according to a second protocol and said second transmitter receiving frame data according to the second protocol;

a second inbound interface which receives frame data output by said second port logic; and

a second outbound interface which outputs frame data to be transmitted to said second port logic, said second inbound interface and said second outbound interface being connected to said interprocessor high-speed interconnect.

13. (original) The system recited in claim 12, further comprising a phase locked loop supplying clock signals to said receiver and said transmitter.

14. (original) The system recited in claim 2, further comprising:

built-in monitors for examining activity of hardware resources; and

means for re-allocating workload to resources that are not heavily utilized.

15. (original) The system recited in claim 14, wherein the built-in monitors examine work queues of said programmable processors.

16. (original) The system recited in claim 14, wherein the built-in monitors examine memory resources of said programmable processors.

17. (original) The system recited in claim 14, wherein the built-in monitors examine interconnection resources of said plurality of programmable processors.

18. (canceled)

19. (new) The system recited in claim 1, wherein the protocol conversion of data frames is performed such that related data frames are dispatched to the same thread unit.

20. (new) The system recited in claim 1, wherein the system converts between two protocols, and the system comprises four processors, and wherein:
a first processor provides inbound processing for a first protocol;
a second processor provides outbound processing for the first protocol;
a third processor provides inbound processing for a second protocol; and
a fourth processor provides outbound processing for the second protocol.